REMARKS/ARGUMENTS

Claims 1-3, 5-39, 41, 49-51 and 53-54 remain in the present application, of which claims 1, 22 and 41 are independent. Claims 1, 2, 5, 9, 14, 20-39, 41, 51 and 53 are amended herein. No new matter has been added. Claim 52 is cancelled without prejudice herein. Applicants respectfully request reconsideration and allowance of claims 1-3, 5-39, 41, 49-51 and 53-54.

I. Rejection of Claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35, 36, 39, 41 and 50-54

Claims 1, 5, 6, 9-11, 14-17, 20-22, 24, 26, 27, 30-32, 35, 36, 39, 41 and 50-54 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 5,909,559 ("So"). Since claim 52 has been cancelled herein, its rejection is now moot.

On pages 8-9 of the Office Action, in rejecting claim 41, the Examiner contends that "So discusses two MPEG streams, audio and video . . . Thus, a transport processor is in the MPEG coder/decoder to allow both streams to be processed," and cites Col. 133, line 62 of So. Applicants respectfully traverse as follows.

In Col. 133, line 60-62, So merely recites, "[a] second VSP block 620 virtualizes 3D audio, graphics, slope/setup and MPEG audio/video compression/decompression." As such, applicants do not see any disclosure of "an MPEG Transport processor for receiving a plurality of MPEG Transport streams" in this section

of So. In fact, So does not disclose any MPEG Transport processor or MPEG Transport streams.

While an MPEG Transport stream may include MPEG video data, not all MPEG video data is carried by an MPEG Transport stream, nor is an MPEG Transport stream required for compression/decompression of MPEG audio/video data. In fact, the term "MPEG Transport stream" has a particular meaning that is well known to those skilled in the art. The MPEG Transport streams are suited for transmission in which there may be potential packet loss or corruption by noise, and/or where it is desirable to send more than one program at a time. As such, an MPEG Transport stream is typically used for broadcasting MPEG data over, for example, satellite and/or cable links.

Each MPEG Transport stream consists of a plurality of Transport packets, which may include packets containing video data, audio data and/or other digital data. The Transport packets in each MPEG Transport stream are formed from MPEG packetized elementary stream (PES) packets, where each PES packet is broken into Transport packets that are multiplexed with the Transport packets formed from other PES packets to form the MPEG Transport stream. As such, an MPEG Transport stream is different from MPEG program streams, which may be formed by multiplexing PES packets having the same time base that are not broken into Transport packets. The MPEG program streams are typically used for transmission in relatively error-free environment and enable easy software processing of the received data.

In addition, MPEG video/audio data may also be carried by MPEG 1 streams (e.g., used in older video compact disks (VCDs)) as well as other streams in vendor specific formats such as, for example, Apple® Quicktime® and Microsoft®'s Active Streaming Format (ASF). Therefore, the disclosure in So that "[a] second VSP block 620 virtualizes . . . MPEG audio/video compression/decompression" does not disclose any MPEG Transport processor or MPEG Transport streams, and should not be construed as such.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Therefore, all claim elements, and their limitations, must be found in the prior art reference to maintain a rejection based on 35 U.S.C. §102.

Since So does not disclose at least "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data," So does not disclose all elements of claim 41. Therefore, So does not anticipate claim 41. Therefore, applicants request that the rejection of claim 41 be withdrawn and that it be allowed.

Since claims 5, 6, 9-11, 14-17, 20-21, 50, 53 and 54 depend, directly or indirectly, from claim 41, they each incorporate all the terms and limitations of claim 41 in

addition to other limitations, which together further patentably distinguish them over the cited references.

By way of example, in rejecting claim 20 on page 6 of the Office Action, the Examiner contends "HDTV means high definition TV which is inferred by referenced to television," and cites Col. 129, line 31 of So. However, Col. 129, line 31 of So merely recites "a television set enclosure" without referring to whether any video is provided having SDTV, HDTV or any other format. Applicants submit that a reference to a television set enclosure does not disclose or even suggest HDTV, much less "the video includes at least one HDTV video," where the HDTV video has been generated by processing the MPEG video data using "an MPEG video decoder for processing the MPEG video data to generate video for displaying."

Further, processing HDTV MPEG-2 video is substantially more difficult than processing standard definition (i.e., compatible with conventional TV) MPEG-2 video. Therefore, even if one were to assert that "TV" somehow implies "HDTV," a system that performs only SD processing does not teach how to perform HD processing. It is not a trivial matter to convert an SD video processor to an HD video processor.

Since claims 5, 6, 9-11, 14-17, 20-21, 50, 53 and 54 are patentably distinguishable over the cited references, applicants request that the rejection of claims 5, 6, 9-11, 14-17, 20-21, 50, 53 and 54 be withdrawn and that they be allowed.

Claim 22 recites, in a relevant portion, "coupling the CPU to a plurality of peripheral devices via a system bridge controller having a north bridge function implemented on an

integrated circuit chip; receiving a plurality of MPEG Transport streams using an MPEG Transport processor implemented on the integrated circuit chip, at least one of the MPEG Transport streams including MPEG video data; and decoding the MPEG video data using an MPEG video decoder implemented on the integrated circuit chip to generate video for displaying." For at least the reasons that are substantially the same as those given above in reference to claim 41, So does not teach all elements of claim 22, and does not anticipate claim 22. Therefore, applicants request that the rejection of claim 22 be withdrawn and that it be allowed.

Since claims 24, 26, 27, 30-32, 35, 36, 39 and 51 depend, directly or indirectly, from claim 22, they each incorporate all the terms and limitations of claim 22 in addition to other limitations, which together further patentably distinguish them over the cited references.

By way of example, claim 30, in addition to all the terms and limitations of claim 22, recites in a relevant portion, "coupling the CPU to one or more I/O devices, the I/O devices being coupled to the integrated circuit chip via a bus different from a PCI bus." Further, claim 51 recites, for the I/O devices coupled to the integrated circuit chip via a bus different from a PCI bus (since claim 51 depends from claim 30), "automatically converting a data access with the first data width by the CPU into multiple data accesses with the second data width to support said at least one of the one or more I/O devices having the second data width." These additional limitations of claims 30 and 51 are not disclosed by So, for example.

For further example, claim 37 recites, in a relevant portion, "coupling the CPU to at least one of the one or more internal components comprises performing format conversion between big-endian data used in the CPU and little-endian data used in the MPEG video decoder," and claim 38 recites, in a relevant portion, "coupling the CPU to at least one of the one or more internal components comprises performing format conversion between little-endian data used in the CPU and big-endian data used in the MPEG video decoder." It can be seen in these claims that the internal components can have opposite endian-ness to the CPU and/or the operating system. Applicants submit that the cited sections of So and Yee et al. do not disclose such conversion of the little or big endian format data between the CPU/operating system and internal components such as an MPEG video decoder.

Since claims 24, 26, 27, 30-32, 35, 36, 39 and 51 are patentably distinguishable over the art of record, applicants request that the rejection of claims 24, 26, 27, 30-32, 35, 36, 39 and 51 be withdrawn and that they be allowed.

Claim 1 has been amended herein to recite, in a relevant portion, "an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data; an MPEG video decoder for decoding the MPEG video data using an external memory to generate video for displaying; a display engine for processing graphics to be blended with the video using the external memory; and a system bridge controller having a north bridge function disposed between a CPU and a plurality of peripheral devices for

coupling the CPU to the plurality of peripheral devices . . . wherein the external memory has a unified memory architecture, such that the external memory is concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video data." (Emphasis Added)

Hence, claim 1 is directed to a single integrated circuit chip comprising an MPEG Transport processor, an MPEG video decoder and a system bridge controller having a north bridge function, and is therefore patentably distinguishable over So for at least the reasons that are substantially the same as those given above in reference to claim 41.

Claim 1 further recites that "the external memory [having a unified memory architecture] is concurrently used by the CPU . . . the display engine . . . and the MPEG decoder . . ." Such external memory having a unified memory architecture, for example, is shown and described in the specification on page 105, line 10 through page 116, line 16 of the specification and FIGs. 32-36 of the application as filed. The memory interfacing of the system bridge controller is described, for example, on page 185, line 17 through page 186, line 29 of the specification as filed. The external memory having a unified memory architecture, such that the external memory is "concurrently used by the CPU through the system bridge controller as at least a part of its main memory, the display engine for processing the graphics, and the MPEG decoder for decoding the MPEG video

data," is further supported, for example, by the specification on page 189, lines 30-36.

So does not disclose such external memory having a unified memory architecture in addition to not disclosing other features such as, for example, "an MPEG Transport processor for receiving a plurality of MPEG Transport streams." Therefore, So does not anticipate claim 1. Therefore, applicants request that the rejection of claim 1 be withdrawn and that it be allowed.

II. Rejection of Claims 2, 3, 7, 8, 12, 13, 15, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 under 35 U.S.C. § 103(a)

Claim 15 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over So. Since claim 15 indirectly depends from claim 41, it incorporates all the terms and limitations of claim 41 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants request that the rejection of claim 15 be withdrawn and that it be allowed.

Claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over So in view of U.S. Patent No. 6,466,581 ("Yee et al.").

Yee et al. is being cited for the proposition that it teaches "converting from little endian to big endian and from big endian to little endian at a PCI controller in order to allow a PowerPC to have access to peripheral devices such as a memory using different endian." The Examiner cites Col. 4, lines 30-48 of Yee et al. to support this allegation.

However, Col. 4, lines 30-48 of Yee merely recites:

> The multimedia computer system 102 includes . . . The host CPU 104 and the host buffer 106 are coupled to a host bus 108, such as a PCI bus or other suitable bus. As known in the art, the host CPU stores the multistream data in memory buffers in independent sizes . . . The on-demand bus master interface controller 100 independently requests multistream data from the buffer 106 in variable length multistream data packets without interrupting processing by the host processor 104 between independent requests for data packets. Preferably, the variable length multistream data packets are shorter than . . .

Applicants do not see how the above-recited Col. 4, lines 30-48 of Yee et al. can be construed to be disclosing conversion between big-endian and little-endian data. Further, Yee et al. does not teach or suggest "an MPEG Transport processor for receiving a plurality of MPEG Transport streams" or that "the external memory has a unified memory architecture."

In order to establish a *prima facie* case of obviousness, in addition to meeting all other requirements, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Since So and Yee et al. together do not teach or suggest "an MPEG Transport processor for receiving a plurality of MPEG Transport streams" or that "the external memory has a unified memory architecture," and the section of Yee et al. cited by the Examiner does not discloses conversion between big-endian data and little-endian data, Yee et al. does not overcome the deficiency of So to reject claims 22 and 41. Therefore, So and Yee et al. together fail to establish a *prima facie* case of obviousness for claims 22 and 41. Therefore,

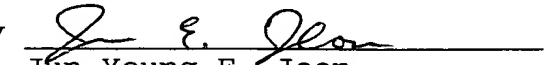
claims 22 and 41 are patentably distinguishable over So and Yee et al.

Since claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 depend, directly or indirectly, from claims 22 and 41, respectively, they incorporate all the terms and limitations of the respective base claim in addition to other limitations, which together further patentably distinguish them over the cited references (including So and Yee et al.). Therefore, applicants request that the rejection of claims 2, 3, 7, 8, 12, 13, 18, 19, 23, 25, 28, 29, 33, 34, 37, 38 and 49 be withdrawn and that they be allowed.

III. Concluding Remarks

In view of the foregoing amendments and remarks, applicants respectfully request an early issuance of patent with claims 1-3, 5-39, 41, 49-51 and 53-54. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call applicants' attorney at the number listed below.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By 
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